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SEP 22 2005
PATENT & TRADEMARK OFFICE

ATTORNEY'S DOCKET NO.: S1022.81112US00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Sylvie WUIDART and Claude ZAHRA	
Serial No.:	10/766,333	Patent No. 6,937,049 B2
Filed:	January 28, 2004	Issued: August 30, 2005
For:	PARALLEL TESTING OF INTEGRATED CIRCUITS	

Examiner:	Trung Q. Nguyen		
Art Unit:	2829	Confirmation No.	3276

ATTN: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Certificate
SEP 28 2005
of Correction

Sir/Madam:

Transmitted herewith for filing is/are the following document(s):

[X] Request for Certificate of Correction
[X] Copies of Page 5 Apl as filed;Page 3 12/01/04 Amn; Page 2 of the NOA and Columns 3 and 6 of U.S. Patent No. 6,937,049
[X] PTO Form SB/44
[X] Return Postcard

If the enclosed papers are considered incomplete, the Mail Room and/or the Application Branch is respectfully requested to contact the undersigned collect at (617)646.8000, Boston, Massachusetts.

No check is enclosed. If it is determined that a fee is necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825. A duplicate of this sheet is enclosed.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on September 19, 2005.

Respectfully submitted,

Sylvie Wuidart et al., Applicant

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Attorney Docket No.: S1022.81112US00
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P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE
OF CORRECTION UNDER 37 C.F.R. §1.322

Sir/Madam:

Patentees respectfully request correction of the above-captioned patent. Specifically, there is typographical errors in column 3 claim 7 and an error of omission in claim 11 of issued U.S. Patent No. 6,937,049.

Patentees submit below a reproduction of column 3, paragraph 9, lines 44-51 of U.S. Patent No. 6,937,049.

> The tester sends, to all chips and after expiry of a time interval At from step 20, an answer request (block 23, SEND CTRL2). Control signal CTRL2 arrives simultaneously on all chips which then respond synchronously (block 24, SEND ANSW) to the tester, that is, synchronized on the tester clock. As soon as they have answered, each of the chips leaves the synchronous operating mode (block 25, SYNC OUT) . (Emphasis added)

Below is a reproduction of the corresponding text found on page 5, lines 6-10 of the application as filed,

> The tester sends, to all chips and after expiry of a time interval Δt from step 20, an answer request (block 23, SEND CTRL2). Control signal CTRL2 arrives simultaneously on all chips which then respond synchronously (block 24, SEND ANSW) to the tester, that is, synchronized on the tester clock. As soon as they have answered, each of the chips leaves the synchronous operating mode (block 25, SYNC OUT). (Emphasis added)

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As originally filed, the time interval was identified on page 5, line 6, as "Δt". However, in the issued patent this time interval was erroneously identified as "At". No such amendment was made by either the Examiner or by Patentees that would change the symbol "Δ" to the letter "A".

Claim 7 as it appears in the amendment filed December 1, 2004 is reproduced below.

7. A method for testing in parallel several integrated circuit chips designed for asynchronous operation, using two physical contacts between a tester and each of the chips, comprising:

transmitting, from the tester a first test control signal to the integrated circuit chips;

having the test executed by each of the integrated circuit chips without synchronizing operation of the integrated circuit chips;

transmitting, from the tester, after a time interval following the transmission of the first test control signal, a second result request control signal to the integrated circuit chips; and

having all chips respond synchronously upon reception of said second control **signal**. (Emphasis added)

The last word in claim 7 as it appears in issued U.S. Patent No. 6,937,049 reads "signa" this is obviously a typographical error that should be corrected to read --signal--.

Claim 11 was amended as shown below by Examiner's amendment on page 2 of the Notice of Allowance.

11. A system for testing a set of identical integrated circuit chips in parallel, comprising:

a plurality of physical contact pairs intended to contact pads of the respective chips; and

for

~~a device capable of:~~

transmitting, ~~from the tester~~ <u>from a tester</u> a first test control signal to the integrated circuit chips;

having the test executed by each of the integrated circuit chips without synchronizing operation of the integrated circuit chips;

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transmitting, from the tester, after a time interval following the transmission of the first test control signal, a second result request control signal to the integrated circuit chips; and

having all chips respond synchronously upon reception of said second control signal.

In support of this request Applicants enclose herewith highlighted copies of: 1) page 5 of the application as filed; 2) page 3 of the amendment filed December 1, 2004; 3) page 2 of the Notice of Allowance; 4) columns 3 and 6 of U.S. Patent No. 6,937,049 and PTO form SB/44.

The corrections requested do not involve change in the patent that constitutes new matter or would require reexamination. Therefore, it is respectfully requested that the correction be made and that a Certificate of Correction be issued.

Patentees respectfully submit that, since the errors for which a Certificate of Correction is sought was the result of Patent Office mistake, no fee is due. However, if the Examiner deems a fee necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825.

Should any questions arise concerning the foregoing, please contact the undersigned at the telephone number listed below.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on September 19, 2005.

Respectfully submitted,

Sylvie Wuidart et al., Applicant

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Attorney Docket No.: S1022.81112US00
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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,937,049

DATED : August 30, 2005

INVENTOR(S) : Sylvie Wuidart and Claude Zahra

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 3, line 45 should read:

--interval Δt from step 20, an answer request (block 23, SEND--

Col. 6, line 32 should read:

--said second control signal--

Col. 6, lines 43-48 should read:

11. --A system for testing a set of identical integrated circuit chips in parallel, comprising: a plurality of physical contact pairs intended to contact pads of the respective chips; and for transmitting, from a tester a first test control signal to--

MAILING ADDRESS OF SENDER

PATENT NO. 6,937,049

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a device capable of implementing the method of claim 1.

6. (Original) The system of claim 5, wherein each integrated circuit chip to be tested is capable of interpreting at least one control signal to switch to a synchronous operating mode.

7. (New) A method for testing in parallel several integrated circuit chips designed for asynchronous operation, using two physical contacts between a tester and each of the chips, comprising:

transmitting, from the tester a first test control signal to the integrated circuit chips;

having the test executed by each of the integrated circuit chips without synchronizing operation of the integrated circuit chips;

transmitting, from the tester, after a time interval following the transmission of the first test control signal, a second result request control signal to the integrated circuit chips; and

having all chips respond synchronously upon reception of said second control signal.

8. (New) The method of claim 7, wherein the time interval is selected to be longer than the maximum execution time of the test steps by any integrated circuit chip.

9. (New) The method of claim 7, wherein an integrated circuit chip receiving said first control signal sets, after execution of the test steps, to a state ready to accept a synchronized answer control signal.

10. (New) The method of claim 7, wherein the test is considered as being negative as soon as the expected binary answer differs from a data word stored on the tester side.

11. (New) A system for testing a set of identical integrated circuit chips in parallel, comprising:

a plurality of physical contact pairs intended to contact pads of the respective chips; and

a device capable of:

transmitting, from the tester a first test control signal to the integrated circuit chips;

a test start control signal comprising, according to the present invention, a request for acceptation of a synchronous operation. On the side of chip 1, the actual test is performed (block 21, PROCESS1) asynchronously (each chip being rated by its own clock) before the chips all set to wait for an answer request control signal coming from the tester (block 22, WAIT CTRL2).

The tester sends, to all chips and after expiry of a time interval Δt from step 20, an answer request (block 23, SEND CTRL2). Control signal CTRL2 arrives simultaneously on all chips which then respond synchronously (block 24, SEND ANSW) to the tester, that is, synchronized on the tester clock. As soon as they have answered, each of the chips leaves the synchronous operating mode (block 25, SYNC OUT).

On the tester side, the synchronously-received answers are interpreted (block 26, INTERP). Since the tester has as many inputs-outputs as it can test chips per batch, the answers received in parallel are interpreted for the different chips which are recognizable (for example, by their position in the batch). In practice, the testing of a chip is considered as being negative as soon as the expected binary answer differs from a predetermined data word stored on the tester side. Since this is an operation verification test, it is enough for one of the chips not to operate properly for it to be declared faulty and to undergo an adequate rejection procedure.

The batch processing enables saving significant time with respect to a series testing since it is performed in parallel on all chips in the batch. All the defective chips are identified and eliminated as with a conventional rejection procedure.

Fig. 5 illustrates the implementation of the test method of the present invention on the integrated circuit chip side.

When supplied, the integrated circuit chip of a transponder expects to receive a control signal and to interpret it. The supply conventionally comes from the electromagnetic radiation of a read/write terminal in the case of a contactless transponder. This especially is one of the functions of the resonant circuit, which is to capture this power. In a test phase, the power is provided similarly by a remote supply carrier by means of contacts 3 and 4.

In its waiting phase, the chip periodically tests the reception of a control signal

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DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

In claim 11, line 3, ";and" has been changed to –and for–; line 4, "a device capable of " has been deleted; line 5, "from the tester" has been changed to – from a tester--.

Allowable Subject Matter

2. Claims 1-12 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: claims 1, 5, 7 and 11 recite, inter alia, "A method for testing in parallel several identical integrated circuit chips with an asynchronous operation, transmitting on the tester side, after a predetermined time interval following the transmission of the first control signal, a second result request control signal to the integrated circuit chips; and having all chips respond synchronously upon reception of said second control signal."

The art of record does not disclose the above limitations, nor would it be obvious to modify the art of record so as to include the above limitations. Although Kim (U.S. 6,359,826) disclose a Method and a system for controlling a

A feature of the present invention is to provide, on the integrated circuit chip side, a specific control signal allowing it to switch to a synchronous operating mode, this control signal being different from an actual synchronization signal (clock).

Another feature of the present invention is that the transmission of this specific control signal comes from the tester and is sent in parallel onto several chips.

FIG. **3** illustrates, in the form of functional blocks, an embodiment of the present invention.

According to the present invention, several chips **1** are connected in parallel by pairs of respective points **3**, **4** to a test device **6** (TEST). Thus, device **6** comprises as many contacts (tips) and inputs-outputs as there are chips to be processed in parallel.

Conventionally, the test which is desired to be performed on the chips is a functional test in radiofrequency mode, that is, test device **6** is intended to emulate the presence of a resonant circuit connected to terminals **11** and **12** of each integrated circuit **1**.

Although this is not shown in the drawings, the test according to the present invention is more specifically intended to be performed on wafers, that is, before cutting of integrated circuit chips **1** for assembly either in cards, or in packages. The number of chips tested in parallel however does not necessarily correspond to the number of chips in a wafer.

FIG. **4** illustrates an embodiment of the test method according to the present invention. This drawing shows in its left-hand portion the steps implemented on the tester side (TESTER) and on its right-hand side the steps implemented on the integrated circuit side (IC).

A test procedure starts according to the present invention with the sending of a control signal CTRL1 (block **20**, SEND CTRL1) in parallel to all integrated circuit chips. Control signal CTRL1 is interpretable by the different integrated circuit chips as a test start control signal comprising, according to the present invention, a request for acceptation of a synchronous operation. On the side of chip **1**, the actual test is performed (block **21**, PROCESS1) asynchronously (each chip being rated by its own clock) before the chips all set to wait for an answer request control signal coming from the tester (block **22**, WAIT CTRL2).

The tester sends, to all chips and after expiry of a time interval Δt from step **20**, an answer request (block **23**, SEND CTRL2). Control signal CTRL2 arrives simultaneously on all chips which then respond synchronously (block **24**, SEND ANSW) to the tester, that is, synchronized on the tester clock. As soon as they have answered, each of the chips leaves the synchronous operating mode (block **25**, SYNC OUT).

On the tester side, the synchronously-received answers are interpreted (block **26**, INTERP). Since the tester has as many inputs-outputs as it can test chips per batch, the answers received in parallel are interpreted for the different chips which are recognizable (for example, by their position in the batch). In practice, the testing of a chip is considered as being negative as soon as the expected binary answer differs from a predetermined data word stored on the tester side. Since this is an operation verification test, it is enough for one of the chips not to operate properly for it to be declared faulty and to undergo an adequate rejection procedure.

The batch processing enables saving significant time with respect to a series testing since it is performed in parallel on all chips in the batch. All the defective chips are identified and eliminated as with a conventional rejection procedure.

FIG. **5** illustrates the implementation of the test method of the present invention on the integrated circuit chip side.

When supplied, the integrated circuit chip of a transponder expects to receive a control signal and to interpret it. The supply conventionally comes from the electromagnetic radiation of a read/write terminal in the case of a contactless transponder. This especially is one of the functions of the resonant circuit, which is to capture this power. In a test phase, the power is provided similarly by a remote supply carrier by means of contacts **3** and **4**.

In its waiting phase, the chip periodically tests the reception of a control signal CTRL1 (block **30**, CTRL1?). It is considered that the selection of the test mode has already been performed upstream and only the instructions likely to occur in test mode are thus considered hereafter.

If the result of test **30** indicates the presence of test instruction CTRL1, the integrated circuit chip sets, as by default, to an asynchronous operating mode (block **33**, ASYNCH). Then, the provided test procedure is executed under the action of control signal CTRL1 (block **34**, PROC). Finally, it sets to a state capable of accepting a synchronization of its operation (block **35**, SYNC AUTH). The chip then sets back to wait for a new instruction.

If a control signal is received, but not instruction CTRL1, the chip then tests whether it is instruction CTRL2 (block **31**, CTRL2?).

In principle, the instruction received after an instruction CTRL1 is instruction CTRL2 transmitted by the tester (block **23**, FIG. **4**). Tests **30** and **31** are then respectively negative and positive. The chip then temporarily sets to a synchronous operating mode (block **36**, SYNC IN) and synchronously sends answer ANSW to the performed test of instruction CTRL1 (block **37**, ANSW PROC). As soon as it has transmitted answer ANSW, the chip resets the authorization for switching to the synchronous mode (block **38**, RESET SYNC AUTH) and returns to the waiting for a next instruction.

If for any reason, the instruction following instruction CTRL1 is not instruction CTRL2, test **31** is negative. This means that the test mode has been left and the chip then does not set to synchronous mode. It directly goes to block **38**, that is, it resets the authorization for switching to the synchronous mode (block **38**, RESET SYNC AUTH) before returning to waiting for a next instruction. The instruction is then processed in synchronous mode as with a conventional instruction.

Similarly, if a control signal CTRL2 is received but it does not follow an instruction CTRL1, test **31** will be positive. However, since the switching to the synchronous mode has not been allowed by procedure **35**, step **36** will be of no effect. Accordingly, there will be no synchronous sending of the chip answer.

An advantage of the present invention is that it respects the secure execution (in asynchronous operation) of the actual test. Indeed, only after the test procedures (block **34**, FIG. **5**) does the chip declare itself ready to accept a synchronous operation control signal. This control signal CTRL2, when received, allows it to synchronously transmit the answer to the test.

It should be recalled that, by default, all processings within a chip of the type to which the present invention applies are processings which are performed in desynchronized fashion, that is, with no link with an external clock.

According to the present invention, only at the end of control signal CTRL2 does the chip switch to a synchronous mode, that is, a mode depending on the external clock.

An advantage of the present invention is that it enables processing several chips in parallel with the test procedure, while respecting a desynchronized processing of the test.

The duration of delay Δt of waiting by the tester between the transmissions of the two control signals is predetermined and selected according to the possible maximum delay of processing of the test instruction by the chips to be tested.

Another advantage of the present invention is that it is perfectly compatible with conventional test procedures and with conventional integrated circuit structures. Indeed, for its implementation, the present invention only requires, from the integrated circuit chip, the understanding of a specific control signal (CTRL2) allowing it to switch to a synchronous operating mode.

Generally, integrated circuit chips to be tested to which the present invention applies are equipped with microcontrollers capable of interpreting different control signals. It is then enough to add a control signal understandable by these microcontrollers.

The practical implementation of the present invention is within the abilities of those skilled in the art based on the functional indications given hereabove. In particular, the modifications to be brought to the integrated circuit chips to be tested according to the needs of the present invention, like for example the addition of a register containing the synchronization authorization indicator (block **35**, FIG. **5**), are within the abilities of those skilled in the art. Further, the determination of the number of chips per batch is within the abilities of those skilled in the art, taking into account, especially, the tester (its capacities of processing the different tests in parallel), the tip board, and the chip size.

Of course, the present invention is likely to have various alterations, modifications, and improvement which will readily occur to those skilled in the art. Such alterations, modifications, and improvements are intended to be part of this disclosure, and are intended to be within the spirit and the scope of the present invention. Accordingly, the foregoing description is by way of example only and is not intended to be limiting. The present invention is limited only as defined in the following claims and the equivalents thereto.

What is claimed is:

1. A method for testing in parallel several identical integrated circuit chips with an asynchronous operation, via two physical contacts between a tester and each of the chips, comprising:

transmitting on the tester side a first test control signal for the integrated circuit chips;

having the test executed in desynchronized fashion by each of the integrated circuit chips;

transmitting on the tester side, after a predetermined time interval following the transmission of the first control signal, a second result request control signal to the integrated circuit chips; and

having all chips respond synchronously upon reception of said second control signal.

2. The method of claim **1**, wherein the predetermined time interval is selected to be longer than the maximum execution time of the test steps by any integrated circuit chip.

3. The method of claim **1**, wherein an integrated circuit chip receiving said first control signal sets, after desynchronized execution of the test steps, to a state ready to accept a synchronized answer control signal.

4. The method of claim **1**, wherein the test is considered as being negative as soon as the expected binary answer differs from a predetermined data word stored on the tester side.

5. A system for testing by twin-wire contact a set of identical integrated circuit chips in parallel fashion, comprising:

a plurality of physical contact pairs intended to contact pads of the respective chips; and

a device capable of implementing the method of claim **1**.

6. The system of claim **5**, wherein each integrated circuit chip to be tested is capable of interpreting at least one control signal to switch to a synchronous operating mode.

7. A method for testing in parallel several integrated circuit chips designed for asynchronous operation, using two physical contacts between a tester and each of the chips, comprising:

transmitting, from the tester a first test control signal to the integrated circuit chips;

having the test executed by each of the integrated circuit chips without the synchronizing operation of the integrated circuit chips;

transmitting, from the tester, after a time interval following the transmission of the first test control signal, a second result request control signal to the integrated circuit chips; and

having all chips respond synchronously upon reception of said second control signa.

8. The method of claim **7**, wherein the time interval is selected to be longer than the maximum execution time of the test steps by any integrated circuit chip.

9. The method of claim **7**, wherein an integrated circuit chip receiving said first control signal sets, after execution of the test steps, to a state ready to accept a synchronized answer control signal.

10. The method of claim **7**, wherein the test is considered as being negative as soon as the expected binary answer differs from a data word stored on the tester side.

11. A system for testing a set of identical integrated circuit chips in parallel, comprising:

a plurality of physical contact pairs intended to contact pads of the respective chips; and

a device capable of:

transmitting, from the tester a first test control signal to the integrated circuit chips;

having the test executed by each of the integrated circuit chips without synchronizing operation of the integrated circuit chips;

transmitting, from the tester, after a time interval following the transmission of the first test control signal, a second result request control signal to the integrated circuit chips; and

having all chips respond synchronously upon reception of said second control signal.

12. The system of claim **11**, wherein each integrated circuit chip to be tested is capable of interpreting at least one control signal to switch to a synchronous operating mode.

* * * * *